Imperial College London

BIOE40002 – Computer Fundamentals and Programming 1

Part I – Digital Logics, Lab 2

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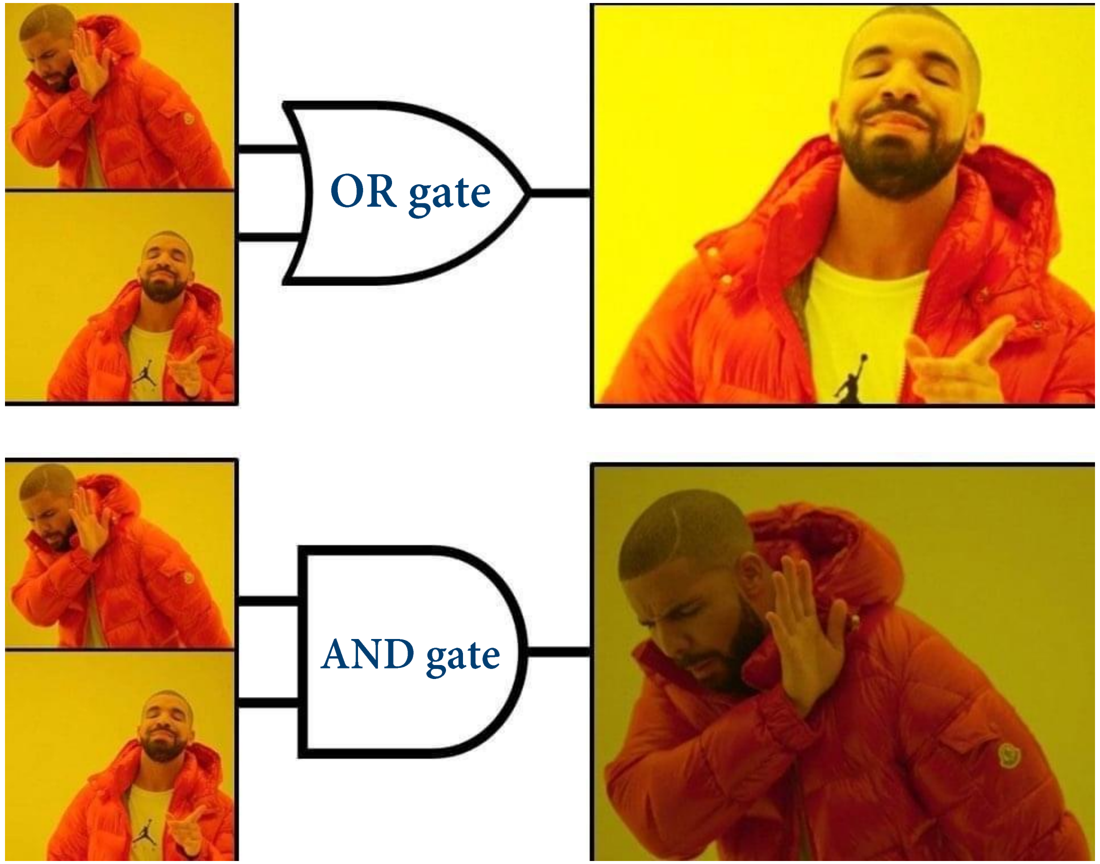
Meme of the day…



Today’s Schedule

- Recap (~ 10 mins)
  - From decimal to binary, binary addition
  - Half adders
  - Full adders
  - From 2-bit adders to 4-bit adders – increase of the bit
- Live demonstration of Quartus Prime Lite
- Lab exercises 6 & 7
- Quiz time !

From decimal to binary

Example: convert $(11)_{10}$ into the binary form

- Step 1: strip down $(11)_{10}$ into the sum of 2^n

$$11 = 1 + 2 + 8 = 2^0 + 2^1 + 2^3$$

- Step 2: express each presented term in 0 or 1

	2^3	2^2	2^1	2^0
Presented?	YES	NO	YES	YES
Binary	1	0	1	1

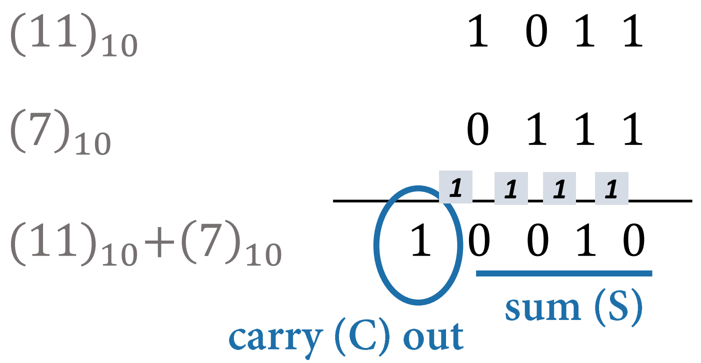
- Therefore, $(11)_{10} = (1101)_2$

To convert decimal to binary:

$$a_n \cdot 2^n + \ldots + a_1 \cdot 2^1 + a_0 \cdot 2^0$$

Binary addition

Example: perform addition $(11)_{10} + (7)_{10}$ in binary

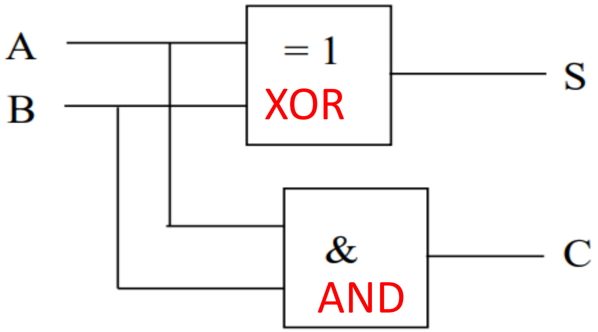


Verify:

$$(11)_{10} + (7)_{10} = \mathbf{18} = (10010)_2$$

Half adders

- *Q:* How to use logic gates to perform binary additions ?
- *A:* Start with 2-bit addition: **a half adder**



A	*B*	*C*	*S*
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	0

Half –No *carry-in* from the previous step (column) can be taken in. It can only stick to the 2-bit additions !

$$\begin{array}{lccc}
(1)_{10} & & 0 & 1 \\
(3)_{10} & & 1 & 1 \\
 & & 1 & 1 \\
\hline
(1)_{10}+(3)_{10} & 1 & 0 & 0
\end{array}$$

Full adders

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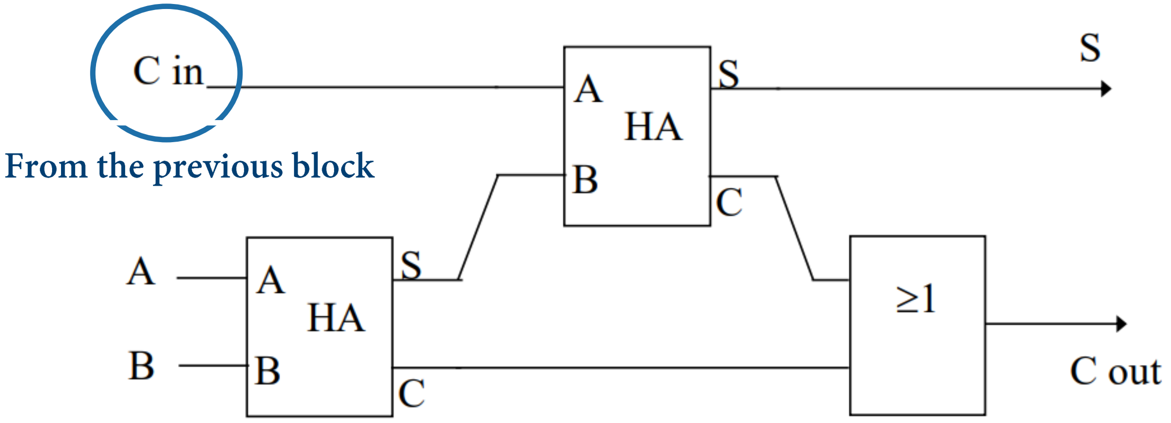
- *Q:* What if we want to perform additions with the carry-in from the previous steps ?
- *A:* try with an intermediate adder !

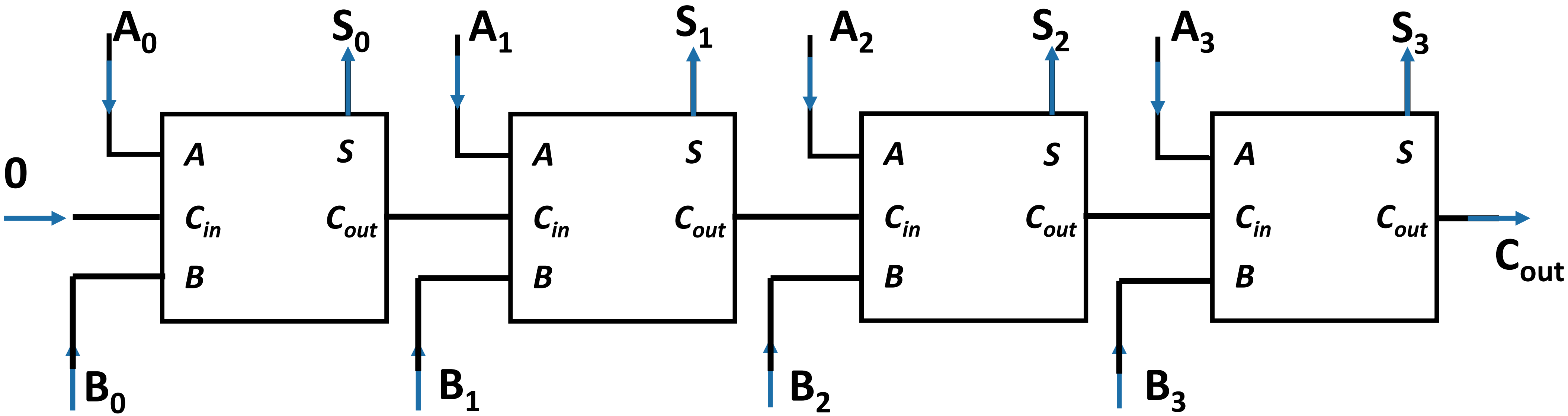


A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- Take a closer look to $\mathrm{C_{in}}$: carry (out) from the last bit (see next slide)

Increase the bit

- In the last 2 slides, we have seen the use of adders for 2-bit additions.
- To increase the bit, we can achieve this by simply connecting full-adders together.



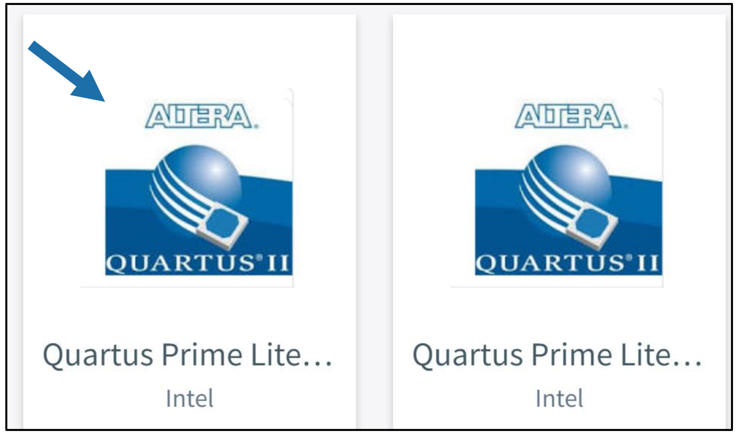
- A 4-bit adder – can evaluate e.g. 1010 + 0011

Questions?

Using Quartus Prime Lite v16.0

- License are required for Quartus Prime Lite users.
- Why bother ? Use college standard set-ups in the Software Hub
  - Need a college VPN to use the Software Hub **on your own PC** –A bit laggy… ?
  - Remote connection to your college account !

- Two versions are available in the Software Hub
  - V 16.0 and V 20.0, very similar features
  - **Go for v16.0 !**



Quartus Prime Lite…
Intel

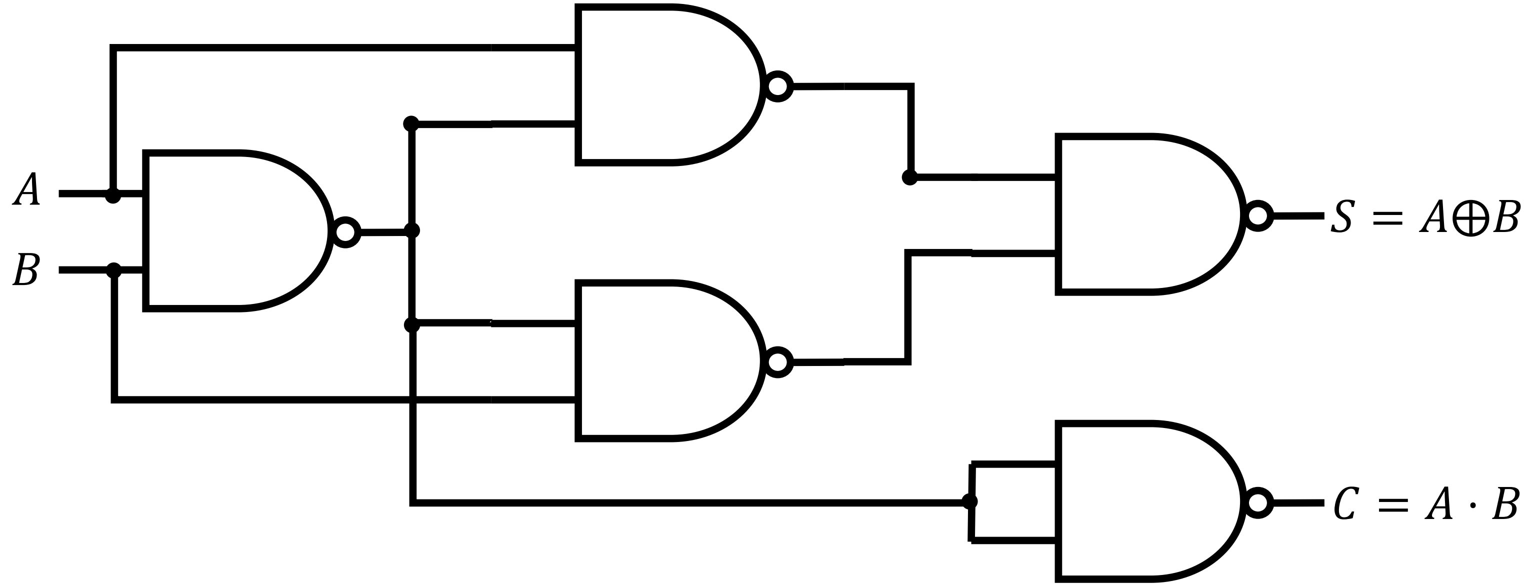
Quartus Prime Lite…
Intel

Questions?

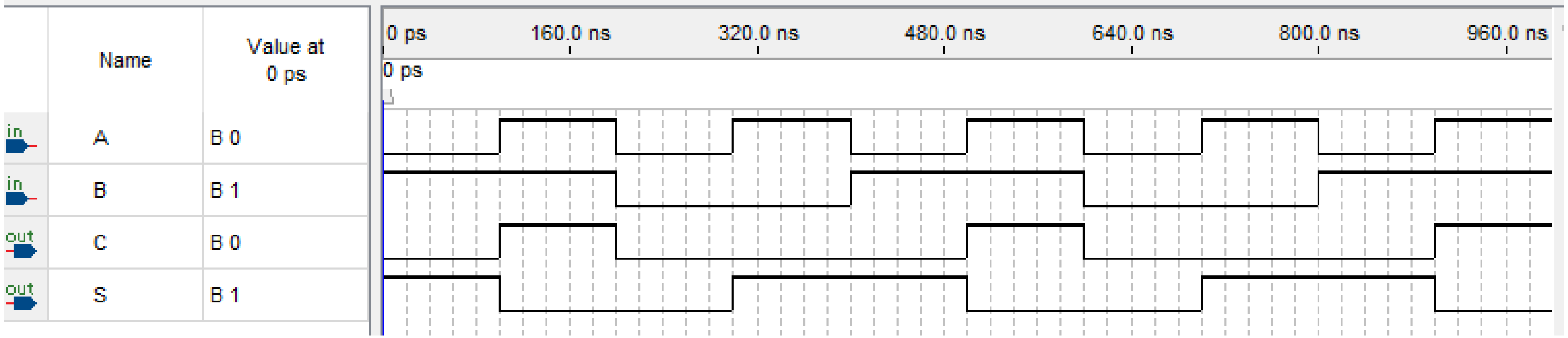
That's it for now.

You can now proceed to the Exercise 6 and 7.

Task 6 – Design a half-adder with *NAND* gates



A	*B*	*C*	*S*
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	0

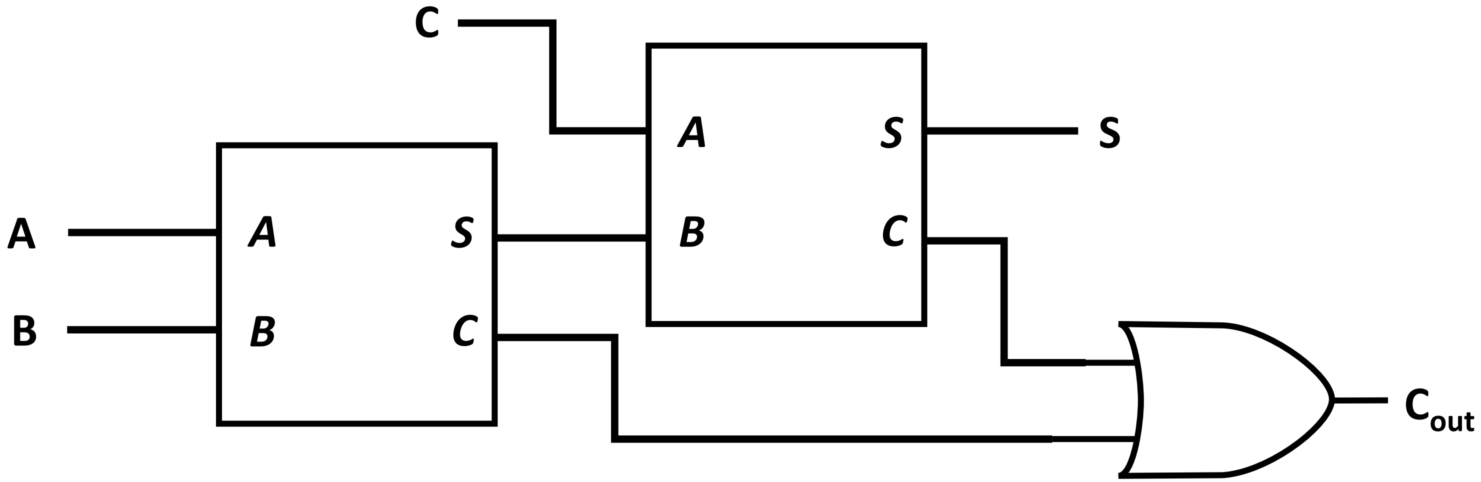


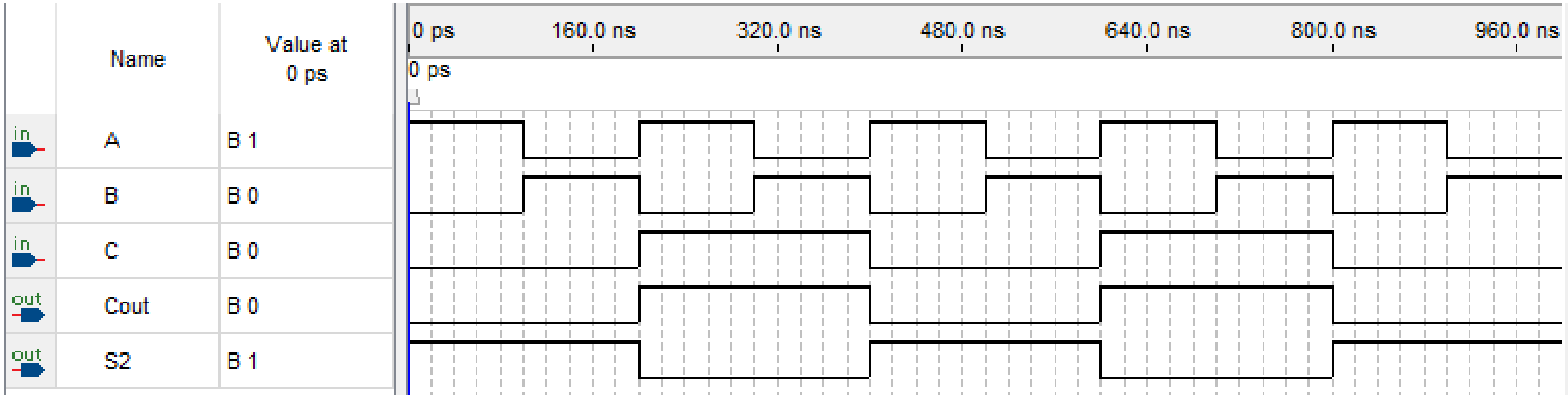
	Name	Value at 0 ps
in	A	B 0
in	B	B 1
out	C	B 0
out	S	B 1

- Grid size = 10ns
- end time = 1us

Task 7 – Design a full adder

- design a full adder with two half adders and an OR gate





	Name	Value at 0 ps
in	A	B 1
in	B	B 0
in	C	B 0
out	Cout	B 0
out	S2	B 1

- Grid size = 10ns
- end time = 1us

Quiz Time!

- *Q1* – One day, when you are having your beef jagga at JCR, a post-doc at EEE comes to you and says that he wants to build some adders. You know he has some real troubles as he was graduated from UCL. As a smart Bioeng student, can you help him to identify which of the following statement(s) regarding adders is/are NOT true?

  a) ***A half adder is constructed with a XOR gate and an OR gate***

  b) ***A full adder is better than half adder as it has a carry out output***

  c) ***A full adder can do multi bit binary addition***

  d) ***A full adder is a combinational logic circuit***

- *Q2* – The next week, the post-doc brings you a 4-bit addition circuit which is assembled by himself. However, the circuit does not work at all. You decide to help him debug. First, you compile a check-list. Which of the following statement(s) from the check-list should be true about a 4-bit addition machine?

    a) ***It requires 4 full adders***

    b) ***It requires 5 full adders***

    c) ***The carry in of the full adder corresponding to the most significant bit is connected to the carry out of the full adder corresponding to the second most significant bit***

    d) ***The carry out of the full adder corresponding to the most significant bit is connected to the carry in of the full adder corresponding to the second most significant bit***

    e) ***None of the above is true***